Electronic Version
Stylesheet Version v1.1.1

[CLOCK SIGNAL AMPLIFYING METHOD AND DRIVING STAGE FOR LCD DRIVING CIRCUIT]

Abstract

A clock signal amplifying method and driving stage for LCD driving circuit is provided. The driving stage includes a clock input, a level shifter, and an output buffer. Firstly, the clock input receives a cock signal oscillating between a high original level and a low original level. Thereafter, a level shifter is biased at a high target level and a low target level, and amplifies the clock signal to a relay signal, which oscillates between a high relay level and a low relay level. Lastly, the output buffer is biased at the high relay level and the low relay level for amplifying the relay signal to a target signal, which oscillates between the high target level and the low target level.